

### **REMARKS**

The present invention is a semiconductor device and a method for forming a capacitor part in a semiconductor substrate. An embodiment of a semiconductor device in accordance with the invention includes a semiconductor base body including a capacitor part A. The capacitor part is buried in a planar semiconductor substrate 10 in a three-dimensional cavity 11 therein. The cavity extends through the substrate by penetrating from a front surface which is to the top of Figs. 1, 2 and 4 to a backside of the substrate. An insulating layer 12 is formed on the front surface and on an inner surface of the cavity 11 as illustrated in Figs. 1, 2 and 4. A laminate structure comprising a first electrode layer 13, a dielectric layer 14 and a second electrode layer 15 is formed inside of the cavity. Each layer is a film. The first electrode layer 13 is exposed from the backside surface of the substrate as illustrated, for example, in Figs. 1(b) and 1(c). The capacitor part includes a concave portion as illustrated, for example, in Figs. 1, 2 and 4.

Claims 4-15 stand objected to on grounds of improper multiple dependency and further, claim 9 stands rejected on grounds of indefiniteness. Newly submitted claims 16-35 have been drafted to overcome the stated grounds of objection and rejection.

Claims 1-4, 7-8 and 10 stand rejected under 35 U.S.C. 102 as being anticipated by United States Patent 5,394,000 (Ellul et al). This ground of rejection is traversed with respect to newly submitted claims 16-35.

Each of the independent claims recites a fundamentally different semiconductor device and a method for forming a capacitor part in a semiconductor

substrate. Each claim includes a capacitor part formed of first, second and third layers with the first layer being a first electrode which is exposed from a backside surface. Ellul et al's capacitor is comprised of a bottom electrode 78, a dielectric layer 88 and a top electrode 90 which are buried in a trench which does not extend through the substrate 60. Neither the first electrode layer 88 nor the second electrode layer 90 extends through the backside as recited in claims 16 and 35. Accordingly, claims 16-35 are not anticipated.

Moreover, there is no basis why a person of ordinary skill in the art would be led to modify the teachings of Ellul et al to arrive at the subject matter of newly submitted claims 16-35.

Claims 1-4, 7-8, 10 and 12 stand rejected under 35 U.S.C. §102 as being anticipated by United States Patent 5,780,335 (Henkels et al). This ground of rejection is traversed with respect to newly submitted claims 16-35.

Similar to Ellul et al, Henkels et al disclose a capacitor fabricated in a trench which does not have an exposed backside electrode as recited in the independent claims. Henkels et al's trench capacitor 12 is formed in a semiconductor substrate 14 as may be seen in Fig. 2c to which the Examiner refers. That capacitor is formed of an inner electrode 16, an insulating layer 20 and an outer electrode 18, all of which are contained within the trench and do not extend through the backside. Accordingly, it is submitted that newly submitted claims 16-35 are not anticipated by Henkels et al.

Moreover, there is no basis why a person of ordinary skill in the art would be led to modify the teachings of Henkels et al to arrive at the subject matter of newly submitted claims 16-35.

Claims 1-10 and 13-15 stand rejected under 35 U.S.C. §103 as being unpatentable over United States Patent 6,184,060 (Siniaguine) in view of United States Patent 5,745,333 (Frankeny et al). The Examiner relies upon the secondary reference of Frankeny et al for comprising a plurality of base bodies. Siniaguine discloses a wafer 104 which includes a silicon substrate which may be "processed to form transistors, capacitors, resistors, conductive lines, and/or other circuit elements, or portions of the circuit elements, in, above and/or below substrate 110" as described in column 2, lines 27-31. However, while Figs. 7-8b and Fig. 10, as referred to by the Examiner do disclose that the wafer 104 may be backside etched to expose the silicon dioxide layer 140 and the metallic layer 150, this structure is not the claimed capacitor part. In fact, this structure is described generally for integrated circuits without any mention being given to components such as capacitors. See column 5, lines 38-56, where dicing of the wafer 104 into different integrated circuits is described, none of which are disclosed as including the claimed capacitor part.

If the proposed combination of Frankeny et al and Siniaguine was made, the claimed subject matter would not be achieved since neither reference teaches the claimed semiconductor device including the claim capacitor part. Moreover, if the combination was made, the result, as described by the Examiner, would be a vertical integrated circuit which would not have the claimed semiconductor part or the method of fabrication thereof including the exposed first electrode layer.

Moreover, the dependent claims define more specific aspects of the present invention which ultimately would not be rendered obvious by the proposed combination of Siniaguine and Frankeny et al.

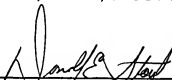
Claim 11 stands rejected under 35 U.S.C. §103 as being unpatentable over Ellul et al in view of United States Patent 4,214,174 (Dickson). This ground of rejection is traversed with respect to newly submitted claims 16-35. The Examiner has cited Dickson for a capacitor structure connected to a clock line. The deficiencies of Ellul et al have been described above with respect to the newly submitted claims 16-35. If the proposed combination was made, Dickson would not cure the deficiencies noted above with respect to Ellul et al with respect to newly submitted claims 16-35.

In view of the foregoing amendments and remarks, it is submitted that each of the claims in the application is in condition for allowance. Accordingly, early allowance thereof is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (892.41103X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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Attachments

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SUBSTITUTE SPECIFICATION

SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1-Field of the Invention

[0001] ———The present invention relates to a semiconductor device employed in DSPs (digital signal micro processors), CPUs (central processing units), memory devices, computer memory, etc., for electronic devices such as computers; and in further detail, it relates to a semiconductor device equipped with a capacitor buried in a semiconductor substrate made from silicon etc.

2-~~Description~~ Description of the Prior Art

[0002] ———With the progress in recent technology, ~~new~~ ~~contents are content~~ is transferred by the technology used for music distribution, animation, true color moving pictures, etc., and the development of electronic devices related thereto is under way. Various technical innovations on devices related to the transfer and/or multimedia in this field are being made.

[0003] ———Concerning technology ~~on~~ regarding integrated circuit design and devices, key items are, for instance, a DSP (Digital Signal Processor), an MPU (Micro Processor Unit), and memory devices (such as ROM and RAM).

Further required on such devices are designs capable of realizing higher control speed, larger memory capacity, and higher stability in performance.

[0004] ——— In order to achieve high speed operation with the semiconductor devices based on IC chips and the like known heretofore, measures have been taken ~~by~~ to directly attaching proper external components such as chip capacitors (decoupling capacitors) to an interposer. Further concerning the internal structure of the semiconductor device, attempts have been made to newly employ copper, which replaces a conventionally used aluminum, as the patterning material for forming circuits.

[0005] ——— However, the semiconductor devices known heretofore failed to sufficiently achieve the requirements concerning, for instance, higher control speed, larger memory capacity, and higher stability in IC performance.

[0006] ——— In semiconductor devices such as IC chips, a wire bonding method is employed in connecting each of the bonding pads (pads for drawing external electrodes), which are provided ~~to~~ for the periphery of the surface of the device, with each of the lead electrodes of the lead frame. In addition to the above, ~~employed are~~ wireless bonding methods are employed for forming joints without using wires, and among them, frequently employed are a flip-chip method using ~~solder~~ solder, bumps, etc., and a TAB method using bump tapes, etc.

[0007] — In Fig. 7 ~~is given~~ a schematically shown external appearance of a DRAM device and a DSP device (60) are illustrated as examples of semiconductor devices known in the art. A signal line is shown by an arrowhead (→) 62, which is externally connected with a chip capacitor (decoupling capacitor) 63, etc. A bonding wire 61 is disposed outward from the periphery of the device 60. Shown aligned therein are plural bonding wires connected to the outside.

#### SUMMARY OF THE INVENTION

[0008] — The present invention has been made in the light of the aforementioned problems of the semiconductor devices known heretofore described above, and a great improvement is made ~~on~~ to the structure and the method of producing the semiconductor devices. The invention provides a key technology for such semiconductor devices, and an object of the present invention is to provide a semiconductor device capable of sufficiently satisfying requirements for future devices such as higher control speed, larger memory capacity, and higher stability in performance, ~~hence, it.~~ Hence, the invention relates to a semiconductor device equipped with a buried type capacitor that is formed by directly burying ~~it~~ the capacitor in a semiconductor substrate (a wafer) made of a material such as silicon and gallium, ~~and the~~ The invention further includes a particularly useful interconnection

technology also useful for semiconductor devices comprising a laminate module (constitution element) having multiple layers on a semiconductor base body or a bare die (exposed chip body), which attains a high precision layer structure and assembly process therefor in semiconductor devices made from materials such as silicon and GaAs.

[0009] — In order to solve the aforementioned problems, the semiconductor device according to the present invention utilizes means as follows. The attached symbols are in conformity with those shown in the drawings.

(1) A three-dimensional cavity 11 is formed aligned in a planar semiconductor substrate 10, a capacitor part A is provided with a capacitor structure of a substrate buried type directly formed by burying ~~this~~ the capacitor structure inside the cavity 11, and semiconductor base bodies (101 - 103) containing the capacitor part A as one constituent, are incorporated to implement a semiconductor device.

(2) In the semiconductor device (1), the capacitor part A is constructed by implementing a capacitor structure comprising a cavity 11 having an aperture (open side) on the surface (device front) 10 of the substrate and extending to an inner part or else reaching the back surface of the substrate.

(3) In the semiconductor device (1) or (2), the cavity 11 is formed and constructed by etching using, for instance, plasma, etc.



(4) In the semiconductor device (1) to (3), an insulator layer 12 such as a silicon oxide film is formed and constructed on the surface (device front) of the semiconductor substrate 10 or on the inner surface of the cavity 11 for passivation.

(5) In the semiconductor device (1) to (4), the capacitor part A is constructed by providing a capacitor structure of a through substrate type cavity, which penetrates inside the substrate 10 from the front surface of the body 10 to the back surface.

(6) In the semiconductor device (1) to (5), the cavity 11 is provided in an approximately truncated cone shape, having a structure with its aperture opened on the front surface (device front) of the body.

(7) In the semiconductor device (1) to (6), a capacitor structure is implemented on the inner surface of the cavity part A by forming a laminated structure of a first electrode layer 13, a dielectric layer 14, and a second electrode layer 15, by means of a thin film deposition method such as CVD, sputtering, electric deposition, spin coating, painting, etc. Further preferably, a sealing material 16, such as polyimide, a metal, etc., is filled inside the concave portion provided on the upper layer of the dielectric layer 14 in the cavity 11.

(8) In the semiconductor device (7), trimming is performed on the dielectric film (dielectric layer) provided in the layer toward the front surface. Trimming refers to controlling the size and the capacity of the dielectric film (dielectric layer)

by using a means such as laser, and this enables adjusting the capacitance to a proper value.

(9) In the constitution of the semiconductor device (1) to (8), the back surface of the substrate 10 at the location of the cavity 11 therein is removed by a means such as etching, etc., such that the device will have an exposed electrode layer 13'.

(10) In the constitution of the semiconductor device (1) to (9), the capacitor part A is arranged so that it can be connected to power source, GNDground, and a signal line.

(11) In the constitution of the semiconductor device (1) to (9), the capacitor part A is arranged so that it can be connected to a clock line.

(12) In the constitution of the semiconductor device (1) to (9), the capacitor part A is placed just under or in the periphery of the input and output pad connected to the substrate.

(13) In the constitution of the semiconductor device (1) to (12), the semiconductor device comprises a laminated module structure containing a plurality of said semiconductor base bodies (110, 111) stacked in layers, and ball bodies (120, 121) are arranged interposed among said semiconductor base bodies (110, 111).

(14) In the semiconductor device (13), the ball bodies (120, 121) have elasticity and they form a cushion structure interposed among said semiconductor base bodies.

(15) In the semiconductor device (13), the ball bodies (120, 121) have electric conductivity and they form an electrically conductive structure interposed among said semiconductor base bodies.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 shows a cross section constitutional view of semiconductor base bodies (101, 102, 103) of a semiconductor device according to the present invention. In the figure, (a) shows a capacitor structure in which the bottom portion of a cavity 11 is provided inside the substrate 10 and not penetrating, (b) shows a capacitor structure in which the first electrode layer (the first metallic layer) provided to the bottom portion side of the cavity 11 is exposed, and (C) shows a capacitor structure in which the cavity has an approximately U-shaped cross section, wherein electrodes ( $\alpha 1$  and  $\alpha 2$ ) are provided to the first electrode layer (first metallic layer), and an electrode ( $\beta 1$ ) is provided to the second electrode layer (second metallic layer).

[0011] Fig. 2 shows an example of a semiconductor device according to the present invention, and provides a cross section view and an upper plan view showing the structure in which a first electrode layer 13 (Ti/W layer, etc.) is formed on the cavity 11.

**[0012]** ——— Fig. 3 shows a semiconductor chip according to an example of a semiconductor device according to the present invention, and is an upper plan view showing a constitution in which a plurality of connection pads (I/O pads) are arranged in the periphery.

**[0013]** ——— Fig. 4 shows an example of the flow of manufacture processes of a semiconductor base body of a semiconductor device according to the present invention, and it provides the process steps showing the procedure of forming a cavity and a capacitor part having a laminate structure.

**[0014]** ——— Fig. 5 shows an arrangement structure showing various arrangements of the capacitor part having a capacitor layered structure in a semiconductor device according to the present invention, wherein (a) is an example in which a plurality of capacitors A are arranged in the periphery of the semiconductor substrate 10, (b) is an example of an arrangement in which the capacitor part A is connected to power source, GND, and signal line, and (c) is an example of an arrangement in which the capacitor part A is connected to a clock line.

**[0015]** ——— Fig. 6 refers to a semiconductor device according to the present invention, and it provides a cross section of an explanatory structure view of interconnection of a plurality of semiconductor base bodies (110, 111) by using ball bodies (120, 121).

[0016] ——— Fig. 7 shows an example of a semiconductor device of a conventional type, and is a schematically drawn outer appearance of a DRAM or a DSP device (60).

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] ——— The mode for implementing the semiconductor device according to the present invention is described in further detail below by making reference to the attached drawings.

[0018] ——— In Fig. 1 is given a cross section view of the constitution showing the semiconductor base bodies (101, 102, 103) constituting the semiconductor device according to the present invention. Referring to the structure shown in Fig. 1 (a), a cavity 11 is formed on the surface of a substrate 10, and the bottom portion of the cavity 11 is inside the substrate 10. Fig. 1 (b) shows a structure in which a means such as etching is applied from the back (bottom) surface of the substrate 10, so that the substrate material is removed, making the substrate thinner in such a manner that the first electrode layer (the first metallic layer) is exposed on the back plane (bottom plane) side of the cavity 11. Further, Fig. 11 (c) shows a capacitor structure having an approximately U shaped cross section, in which electrodes ( $\alpha 1$  and  $\alpha 2$ ) are formed on the first electrode layer (first metallic layer) and an electrode ( $\beta 1$ ) is formed on the second electrode layer (second metallic layer).

[0019] — The cavity 11 formed inside the semiconductor substrate 10 has a three-dimensional structure. As an example of the three-dimensional structure, ~~there can be mentioned a~~ truncated cone shape ~~as is shown in the figure~~, but the shape need not be limited thereto. More specifically, there can be ~~mentioned various types of three-dimensional shapes such as~~ a reverse truncated cone shape, cylindrical shape, dish shape, pot shape, bowl shape, vase shape, conical shape, etc. Furthermore, as the cross section shape of the three-dimensional morphologies above, there can be mentioned shapes such as circular, ellipsoidal, polygonal, and asymmetrical shapes as desired.

[0020] — Referring to Fig. 1, the cavity 11 is of a structure having an aperture or an opening on the substrate 10 (device surface); the enlarged diameter side of the cavity shape has its aperture opened at the surface of the substrate 10, while the shorter diameter side forms a concave shape inside the substrate. In Fig. 1, the entire cavity is shown with an approximately truncated cone shape (reversed conical shape). ~~As a matter of course, the~~ The illustrated three-dimensional morphology ~~not only is not limited thereto, but and also can~~ have an aperture on the surface of the substrate 10 having a diameter smaller than the lateral diameter of the cavity provided inside the substrate. More specifically, for instance, there can be provided a bucket-like morphology or a reversed

bucket-like morphology, or there can be provided a triangular flask morphology or a reversed triangular flask morphology. Furthermore, straight and cylindrical or square trench shaped cavity structures constant in width, which are well known for being the cavity structure of a memory employed in a conventional DRAM device, etc., may be employed as well.

[0021] ——— The cavity 11 comprises, in the concave portion provided to the inner plane thereof, a capacitor part A equipped with a capacitor structure buried in the substrate 10. Firstly, a cavity 11 is formed on the surface of the semiconductor substrate 10 by means of plasma etching, etc. Then, in a passivation process, a silicon dioxide ( $\text{SiO}_2$ ) film 12 is formed on the surface of the semiconductor substrate 10 and on the inner surface of the cavity 11.

[0022] ——— Subsequently, a first electrode layer 13 (such as Ti/W layer, etc.) is formed in the cavity 11 by means of a thin film deposition method such as CVD, sputtering, electric deposition, spin coating, painting, etc., and then, a dielectric layer 14 is laminated thereon by using a dielectric material such as polyimide (PI). Further thereon, a second electrode layer 15 is formed laminated thereon to complete a multilayered laminate structure for capacitor part A.

[0023] ——— Also, a capacitor part having a laminate structure formed by repeating the process steps of forming the first electrode layer 13 through the second electrode layer 15

may be provided. Alternatively, the cavity substrate surface prior to the formation of the first electrode layer 13 or the first electrode layer itself may be surface roughened by means such as sandblasting or etching to increase the area of the capacitance carrying surface, and the dielectric layer 14 and the second electrode layer 15 may be formed thereon, such that the capacitance of the capacitor formed inside the cavity may be increased.

[0024] —Furthermore, preferably, a sealing material 16 such as polyimide, etc., or a metal, etc., may be filled in the concave portion generated on the upper side of the dielectric layer 14 provided inside the cavity 11. In this case, an electrically insulating material is used as the sealing material 16 at the surface in contact with the second electrode layer 15, but it may be formed otherwise by incorporating an insulating film or an insulating layer.

[0025] —In Fig. 1 (c) is shown another example (semiconductor base body 103) of a semiconductor device according to the present invention. The cavity 11 used herein is provided in morphology as such similar to a U-shaped cross section or a vase-like shape, such that the bottom is provided with an edge-free round shape. In this case again, similar to (a) and (b), there is constructed a capacitor part A having a multilayered laminate structure comprising a first electrode layer 13 (e.g., a Ti/W layer, etc.), a dielectric layer 14 (made



of polyimide, etc.), and a second electrode layer 15, and furthermore, the first electrode layer 13 comprises an electrode  $\alpha 1$  on the front surface and an electrode  $\alpha 2$  on the back side, and the second electrode layer 15 comprises an electrode  $\beta 1$  on the front surface. By providing such a structure, the capacitor function of the present invention can be realized by taking  $\alpha 1$  and  $\beta 1$  as electrodes, or  $\alpha 2$  and  $\beta 1$  as electrodes.

[0026] ——— In a common parallel plated capacitor, the capacity  $C$  can be expressed by an equation  $C = \epsilon S/D$ , where  $S$  represents the area of the electrode,  $D$  represents the thickness of the dielectric (distance between the electrodes), and  $\epsilon$  represents the dielectric constant of the dielectric. Thus, as is clearly understood from this equation, in order to increase the capacity  $C$  of the capacitor according to the present invention, it is important to increase the area  $S$  of the electrodes (i.e., the first electrode layer 13 and the second electrode layer 15 in the present invention), while thinning the thickness  $d$  of the dielectric (i.e., the dielectric layer 14 in the present invention) and using a material having a high dielectric constant  $\epsilon$ ).

[0027] ——— In Fig. 2 is shown a semiconductor device according to the present invention, showing the cross section view and the upper plan view of a structure comprising a first electrode layer 13 (e.g., Ti/W layer, etc.) formed inside a cavity 11. The cavity 11 is formed on a substrate 10, and,

in a passivation process, a silicon dioxide ( $\text{SiO}_2$ ) film 12 is formed on the surface of the semiconductor substrate 10 and on the inner surface of the cavity 11. The first electrode layer 13 is formed in such a manner that it may continuously cover both the inner surface of the cavity 11 and the substrate surface at the periphery of the cavity. The first electrode layer 13 shown in Fig. 2 is indicated as a rectangle or a square as seen from above, with the sides x and y thereof decided by taking the size and the shape of the cavity 11 into consideration. Furthermore, the shape of the first electrode layer 13 herein is not only limited to a rectangle or a square as shown in Fig. 2, but may be of any shape such as circle or oval. Further, the depth of the cavity 11 herein may be set approximately equal to the thickness n of the substrate 10 as shown in Fig. 2, because the metallic layer 13' (i.e., the first electrode layer 13) is exposed from the back of the substrate 11. By setting a solder, a bump, etc., on the metallic layer 13' herein and by joining it with an interposer and the like, the connection with the outside may be facilitated.

[0028] ——— In Fig. 3 is shown an upper planar view of a semiconductor chip according to an example of the semiconductor device of the present invention. A silicon substrate 10' is connected in contact with a chip substrate 20, and a pad portion (e.g., 21, 22, etc.) is provided to the periphery thereof. On designing the semiconductor chip here in case of using a silicon

substrate of a proper size, for instance, the thickness of the silicon substrate 10 may be set to approximately 200  $\mu\text{m}$ , and the cavities may be set to 10 - 12 pcs/line  $\times$  4 = 48 pcs [max.], while freely arranging the cavities.

**[0029]** —Referring to Fig. 3, a plurality of pad portions (e.g., 21, 22, etc.) for external connection are arranged on the periphery of the silicon substrate 10'. The pad portions (e.g., 21, 22, etc.) can be formed as capacitors with structure according to the present invention. In accordance with the semiconductor device of the present invention, as shown in Fig. 1 (C), the structure is provided as such that the capacitor electrodes may be taken from the front side (e.g.,  $\alpha 1$  and  $\alpha 2$ ), or one electrode each taken from the front and the back sides (e.g.,  $\alpha 2$  and  $\beta 1$ ) of the substrate. By appropriately combining the electrodes, the electrode (bonding pad) provided to the periphery of the IC chip surface can be connected simply to the lead frame, and this largely contributes to the realization of efficient design, reduced product size, etc., thereby leading to the production of a product matching the market needs.

**[0030]** —Figure 4 is related to the production of a semiconductor device according to the present invention, and shows an example of the process steps for forming a cavity and a capacitor part according to the capacitor laminated structure.

(a) The semiconductor substrate (wafer) 10 is made of a material

such as of silicon, gallium arsenide, etc., and a three-dimensional cavity 11 is formed in such a manner that the aperture is formed on the surface of the substrate. The cavity may be formed by properly selecting a means such as plasma etching, etc. The cavity is aligned and formed by setting, for instance, the morphology, the size, the cavity depth, the number, the interval, and the location, based on the design of the semiconductor device.

(b) A silicon oxide film (e.g.,  $\text{SiO}_2$  layer) 12 is formed on the surface of the semiconductor substrate 10 and on the inner plane of the cavity 11 in a passivation process.

(c) A first electrode layer (a first metallic layer) 13 is formed by attaching Ti/W, etc.

(d) A dielectric layer 14 using a dielectric material such as polyimide (PI) is formed by laminating it on the first electrode layer 13.

(e) A second electrode layer (a second metallic layer) 15 is formed superposed on the first electrode layer (first metallic layer) 13 and the dielectric layer 14.

**[0031]** ————In the process steps (d) or (e), a part or a large part of the first electrode layer 13 may be exposed on the substrate surface in such a manner that an electrode may be connected to the first electrode layer (first metallic layer) 13 provided to the surface of the substrate 10.

[0032] ——— Furthermore, on forming a thin film in the process steps (c), (d), and (e), a means of thin film deposition such as CVD, sputtering, electric deposition, spin coating, painting, etc., may be properly employed.

(f) In this example of this process step, the front surface of the substrate 10 and the surface exposed opposite thereto (i.e., the back or lower surface) at the cavity 11 provided therein are thinned by means of etching, etc., such that a part or the entire surface at the cavity may be removed, exposing the electrode layer 13'. A capacitor part A is formed in this manner. Thus, a first electrode layer (first metallic layer) is exposed at the bottom plane (lower plane) of the cavity 11, and this can be used as the capacitor electrode.

[0033] ——— In Fig. 5 is an structure diagram showing various types of arrangements of a capacitor part A having a capacitor laminate structure of the semiconductor device according to the present invention. Referring to the figure, a filled circle represents an I/O pad (A) comprising a capacitor part in which the capacitor structure according to the present invention is applied, and open circle represents an I/O pad (C) of a conventional type having no capacitor part according to the present invention. The I/O pad (filled circle) (A) according to the present invention may be properly and freely used in combination with the conventional I/O pad (open circle) (C) and arranged on the semiconductor substrate to

constitute various types of semiconductor devices. As the semiconductor substrate, as a matter of course, used are not only those made of silicon, but also substrates made of other materials such as GaAs.

**[0034]** ——— In Fig. 5(a) is shown an example in which a plurality of capacitor parts A according to the present invention are arranged and set in the periphery of the semiconductor substrate 10". The capacitor structure of this type may be set up as a pad portion connected to an interposer etc. Preferably, capacitor parts C of conventional types may be properly combined and arranged on the semiconductor substrate.

**[0035]** ——— The signal quality of the signals provided in the signal line can be improved in this manner by aligning a capacitor structure according to the present invention just under the I/O pad provided in the semiconductor substrate, or in the periphery thereof.

**[0036]** ——— Further, in Fig. 5(b) is shown an example of aligning the capacitor part A according to the present invention in a manner suitable for connection with a power source, GND, and signal line. By aligning the capacitor part A according to the present invention as a decoupling capacitor for the power source - GND line, a semiconductor device assuring an extremely high speed operation can be implemented.

**[0037]** ——— In Fig. 5(c) is shown an example of aligning the capacitor part A according to the present invention in a manner suitable for connection with a clock line. By aligning the capacitor part A to a clock line within the silicon substrate 10" as a capacitor differing in capacitance value, it can greatly contribute to energy management.

**[0038]** ——— The present invention further comprises a particularly useful method of interconnection among base bodies, i.e., the key technology for semiconductor devices, and it provides a technology for forming a laminate module (constitution element) having multiple layers on a base body or an exposed chip body (bare die). Further, this interconnection technology can be effectively applied to the high precision layer structure and the assembly process of semiconductor devices made from semiconductor materials such as silicon and GaAs.

**[0039]** ——— Figure 6 refers to a semiconductor device according to the present invention, and is an explanatory diagram showing the cross section view of the structure of an example for constituting an interconnection structure by using ball bodies (120, 121) placed between a plurality of semiconductor base bodies (110, 111).

**[0040]** ——— The semiconductor device according to Fig. 6 can provide a module structure as a 3D-laminate package in which plural semiconductor base bodies (110, 111) are superposed in

layers, and in this case, the ball bodies (120, 121) are preferably interposed between the capacitor-type through holes (A1-A3, A2-A4) of the semiconductor base bodies (110, 111).

**[0041]** ——— Furthermore, by using a material having elasticity for the ball bodies (120, 121), a cushion structure may be formed among said semiconductor base bodies (110, 111).

**[0042]** ——— Further, said ball bodies (120, 121) may have electric conductivity, such that an electrically conductive structure may be formed between the through holes (A1-A3, A2-A4) of the capacitor parts of said semiconductor base bodies.

**[0043]** ——— By connecting the capacitor type through hole semiconductor base bodies by using elastic solder ball bodies in this manner, a favorable combination structure can be implemented.

**[0044]** ——— As described above, the technology according to the present invention comprising forming an interconnection (an internal connected structure) by using elastic balls that are directly interposed or inserted inside the module (constituent component) is extremely useful for the high precision layer structure and the assembly process of the future semiconductor chips.

**[0045]** ——— In a semiconductor device known heretofore, a protective film was provided on the wafer or the base body, such that the narrow gaps between each of the wafers would be controlled to yield a proper pressure, and there was a



requirement that a precise module must have surface planarity of high precision in the thin film wafers and base bodies. However, in accordance with the present invention, the technology above for maintaining the narrow gaps is no longer necessary. Accordingly, the elastic support structure using the ball bodies is found to be a useful technology in improving future high precision layer structures and the assembly processes.

[0046] ——— As described above, the semiconductor device according to the present invention shows distinguished features, and provides excellent advantages as follows.

(1) The semiconductor device according to the present invention comprises a constitution comprising a capacitor part A buried in a silicon substrate, thereby minimizing the inductor (L component) included in the circuit and realizing a high speed operation. Further, not only silicon substrate materials, but also other materials such as GaAs can be employed for the substrate.

(2) In accordance with the structure and the production process for semiconductor devices of the present invention, when compared with the capacitance (several fF) obtained in the conventional devices employing a trench structure, the semiconductor device according to the present invention can produce a value ranging from several tens of pF to a larger value of several nF with a single cavity.

(3) In accordance with the structure and the production process for semiconductor devices of the present invention, the allowance of the capacitance can be controlled to a margin of error which is only a few percent that of conventional chips.

(4) According to the present semiconductor device, several structural improvements can be made by applying a capacitor structure of the present invention just above or just below, or in the vicinity, of each of the I/O pads on the silicon substrate. Hence, the design and the production of the capacitor can be made extremely reasonably and efficiently, and this largely contributes to the realization of reduced product size, chip size packaging, improved high performance, etc., thereby leading to the production of a product matching the market needs.

(5) In the semiconductor device according to the present invention, the proper value for capacitance can be controlled by trimming the dielectric film (dielectric layer) provided on the layer at the front surface. Trimming refers to a method of controlling the size and the capacitance of the dielectric film (dielectric layer) by using a laser, etc.

(6) In the semiconductor device according to the present invention, if necessary, the electrode of the capacitor formed inside a substrate such as silicon or GaAs can be connected to the signal line (power source, GND, or a signal line) provided just under it.

(7) In the semiconductor device according to the present invention, by providing elastic ball bodies between the semiconductor base bodies, the problem of chipping occurring on thin film wafers and base bodies can be overcome, and mechanical stress can be absorbed by the elastic function of the ball bodies. Furthermore, since the narrow gaps between each of the wafers and bare dies (exposed chip bodies) as well as the self alignment can be easily controlled by the elastic properties and the operation thereof, a semiconductor device of high performance can be easily implemented.

#### ABSTRACT

A semiconductor device equipped with a buried type capacitor directly buried inside a semiconductor substrate, wherein three-dimensional cavities 11 each having an aperture on the front side of the flat semiconductor substrate 10 are formed aligned with each other on the substrate 10, a capacitor part A is provided by implementing a capacitor structure of a substrate-buried type inside the cavity 11, and semiconductor base bodies 101 ~~include these~~ including capacitor parts A, is provided.